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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/632,910	08/04/2000	Kohei Tatsumi	52433/609	1969
26646	7590	02/01/2005	EXAMINER	
KENYON & KENYON ONE BROADWAY NEW YORK, NY 10004			CHAMBLISS, ALONZO	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 02/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/632,910

**Applicant(s)**

TATSUMI ET AL.

**Examiner**

Alonzo Chambliss

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 24 November 2004.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 16-19 and 25 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 16-19 and 25 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 09/254,119.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. The amendment filed on 11/24/04 has been fully considered and made of record in the instant application.

### ***Response to Arguments***

2. Applicant's arguments filed 11/24/04 have been fully considered but they are not persuasive.

Applicant alleges that Juskey does not show a semiconductor device having spherical solder balls. This argument is deemed unpersuasive because Mitchell is relied upon to disclose this feature.

Applicant alleges that Juskey does not show flux as an adhesive for bonding solder balls, which are mobile, in place. This argument is deemed unpersuasive because Juskey discloses using a flux as an adhesive for bonding solder balls to the electrode (see col. 3 lines 26-45; Fig. 3). In regards to the mobility of the metal balls the claims are not so limited in scope.

Applicant alleges that Juskey has no disclosure or suggestion in Fig. 3 of adhesive bonding metal balls to the electrodes of a semiconductor chip with a flux without reflowing the metal balls. This argument is deemed unpersuasive because Juskey discloses that the solder bumps can be used with chip carrier or other member that is well known in the art (see col. 1 lines 13-17). Thus, the solder is reflowed on the chip carrier but is not reflowed when attached to a chip having an electrode and a flux.

Applicant alleges that Juskey does not disclose a spherical ball but a semi-spherical. This argument is deemed unpersuasive because the definition of spherical is having a form of a sphere or of one of its segments. Thus, semi-spherical is considered one of the segments of a sphere.

Applicant alleges that Okuyama is not properly combinable with Juskey. This argument is deemed unpersuasive because Juskey and Okuyama have substantially the same environment of attaching solder balls to a semiconductor device. Regardless of the size of the solder balls Juskey and Okuyama both show effective methods of placing solder balls to a semiconductor device that allow the semiconductor device to be attached to an external semiconductor device. Therefore, it would have been obvious to use vacuum device with Juskey, since the vacuum device would automatically form high density solder bumps and simultaneously mount a plurality of solder bumps on electrode pads of the chip as taught by Okuyama.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of

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the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 16-18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey, Jr. et al. (U.S. 4,940,181) and Mitchell et al. (U.S. 5,773,359).

With respect to Claims 16 and 17, Juskey discloses electrodes 18, 20, 22 formed on a chip carrier substrate 10 (see Figs. 1-3). Juskey discloses that the solder bumps can be used with chip carrier or other member that is well known in the art (see col. 1 lines 13-17). Thus, it would have been obvious to substitute the semiconductor chip in place of the carrier substrate, since a semiconductor chip is formed from a wafer substrate that has been sliced into individual chips. Furthermore, one skilled in the art would readily recognize from Juskey that a flip chip bonding procedure takes place, since flip chip bonding incorporates placing solder balls on a chip and then flipping the chip to a substrate to yield a final product that is seen in Figs. 3 and 4. Juskey discloses adhesively bonding the metal balls to the electrodes with a flux without reflowing the metal balls, whereby the metal balls are only bonded to the electrodes with flux without reflowing (see col. 3 lines 26-40). Each bump 30 consists of a metal ball having a given size, and adhesive bonded to the electrodes 18, 20, and 22 for the

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attachment of the bumps 30. Each electrode 18 includes a layer of an electrode material 20 and at least one layer 22 laminated to the layer of the electrode material 20 to avoid deterioration (i.e. strengthen and protect) bonding such that the at least one layer 22 has a peripheral dimensions substantially the same as those of the electrode material 20. The metal balls 30 are adhesively bonded to the respective electrodes with a flux 26. The metal balls 30 are reflowed. Thus, the metal balls 30 are physically attached to tops of the electrodes 18, 20, and 22 (see col. 2 lines 35-60 and col. 3 lines 33-39; Figs. 2-4). Juskey fails to explicitly disclose a spherical metal ball having a diameter of not greater than 150 micrometers. However, Mitchell discloses a spherical metal ball having a diameter of not greater than 150 micrometers (see col. 3 lines 31-37 and col. 5 lines 33-35). Therefore, it would have been obvious to substitute the smaller spherical diameter ball for the metal balls of Juskey, since the smaller diameter balls would provide a reliable electrically connection between two semiconductor components as taught by Mitchell.

With respect to Claims 18, Juskey discloses applying the flux 26 to the electrodes 18, 20, 22 (see Fig. 3; Col. 3 lines 26-34).

With respect to Claim 25, the bumps 30 consisting of metal balls are adhesively bonded to the respective electrodes 18, 20, 22 on the semiconductor substrate 10 (i.e. semiconductor chip) (see col. 3 lines 26-40; Fig. 4).

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Juskey, Jr. et al. as applied to claim 16 above, and further in view of Okuyama (JP 4-65130).

With respect to Claim 19, Juskey fails to disclose wherein the metal balls are adhesive bonded to the electrodes by a process comprising the steps of applying vibration at a small amplitude to a vessel containing the metal balls to cause the metal balls to jump up. Arranging and holding the metal balls on an arrangement base plate by attracting the jumping up metal balls to attraction openings provided in the arrangement base plate in positions corresponding to the electrodes of the semiconductor chip to which the metal balls are to be adhesive bonded. Removing excess metal balls adhering either to the arrangement base plate or to the metal balls attracted to the attraction openings and simultaneously contacting the metal balls held and arranged on the arrangement base plate with the electrodes of the semiconductor chip. Okuyama discloses wherein the metal balls 8 are adhesive bonded to the electrodes 6 by a process comprising the steps of applying vibration at a small amplitude to a vessel containing the metal balls 8 to cause the metal balls 8 to jump up. Arranging and holding the metal balls 8 on an arrangement base plate 29 by attracting the jumping up metal balls 8 to attraction openings 31 provided in the arrangement base plate 29 in positions corresponding to the electrodes 6 of the semiconductor chip 2 to which the metal balls 8 are to be adhesive bonded. Removing excess metal balls 8 adhering either to the arrangement base plate 29 or to the metal balls 8 attracted to the attraction openings 31 and simultaneously contacting the metal balls 8 held and arranged on the arrangement base plate 29 with the electrodes 6 of the semiconductor chip 2 (see English abstract and all of the figures). Thus, Juskey and Okuyama have substantially the same environment of attaching solder balls to a semiconductor device.

Therefore, it would have been obvious to use vacuum device with Juskey, since the vacuum device would automatically form high density solder bumps and simultaneously mount a plurality of solder bumps on electrode pads of the chip as taught by Okuyama.

The prior art made of record and not relied upon is cited primarily to show the process of the instant invention.

### ***Conclusion***

6. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see <http://pair-dkect.uspto.gov>. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or [EBC\\_Support@uspto.gov](mailto:EBC_Support@uspto.gov).



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A handwritten signature in black ink, reading "Alonzo Chambliss". The signature is written in a cursive style with a large, stylized initial "A".

Alonzo Chambliss  
Primary Patent Examiner  
Art Unit 2814

AC/January 31, 2005